CLAIM AMENDMENT:

Please amend Claims 1, 4, 5, 32, 35, 36, 43, 44, 45, 46, 49, 50, 53 and 54, cancel claims 3 and 34 and add new claims 92 and 93.

Claim 1 (currently amended): A sealing apparatus for sealing a semiconductor wafer having semiconductor elements on its surface by resin, comprising:

an upper mold; and

a lower mold having [[an]] a first area where the semiconductor wafer is to be mounted, wherein the lower mold ~~having~~ has an uneven surface ~~in the area~~ ,which is formed within a second area, which is in the first area, and wherein the uneven surface is not formed in the periphery of the first area.

Claim 2 (original): A sealing apparatus as claimed in claim 1, wherein the uneven surface is formed by an electric discharging process in coarse condition.

Claim 3 (cancelled).

Claim 4 (currently amended): A sealing apparatus ~~as claimed in claim 2,~~ for sealing a semiconductor wafer having semiconductor elements on its surface by resin, comprising:

an upper mold; and

wherein the uneven surface has a roughness in a range between 8μm and 12μm.

Claim 5 (currently amended): A sealing apparatus as claimed in claim [[3]] 2, wherein the uneven surface has a roughness in a range between 8μm and 12μm.

Claim 6 (original): A sealing apparatus as claimed in claim 1, wherein the uneven surface is formed by slits.

Claim 7 (original): A sealing apparatus as claimed in claim 6, wherein the slits are formed in parallel to each other.

Claim 8(original): A sealing apparatus as claimed in claim 6, wherein the area is a first area, the slits is formed within a second area, which is in the first area, and the slits are not extended to the periphery of the first area.

Claim 9 (original): A sealing apparatus as claimed in claim 7, wherein the area is a first area, the slits is formed within a second area, which is in the first area, and the slits are not extended to the periphery of the first area.

Claim 10 (original): A sealing apparatus as claimed in claim 1, wherein the uneven surface is formed by a single spiral slit.

Claim 11 (original): A sealing apparatus as claimed in claim 10, wherein the area is a first area, the single spiral slit is formed within a second area, which is in the first area, and the single spiral slit is not extended to the periphery of the first area.

Claim 12 (original): A sealing apparatus as claimed in claim 1, further comprising a shock absorber, which is formed under the lower mold, buffering stress from the upper mold when the semiconductor wafer is sandwiched by the upper and lower molds.

Claim 13 (original): A sealing apparatus as claimed in claim 1, further comprising shock absorbers which are formed under the lower mold, buffering stress from the upper mold when the semiconductor wafer is sandwiched by the upper and the lower mold, the shock absorbers being disposed symmetrically against the center of the area.

Claim 14 (original): A sealing apparatus as claimed in claim 12, wherein the shock absorber is formed by a metallic compression spring.

Claim 15 (original): A sealing apparatus as claimed in claim 13, wherein each shock absorber is formed by a metallic compression spring.

Claim 16 (original): A sealing apparatus as claimed in claim 12, wherein the shock absorber is a first shock absorber, further comprising:

a first block having a first recess, the lower mold being contained in the first recess;

a second block having a second recess, the first block being contained in the second recess; and

a second shock absorber, which is formed under the second block, buffering stress from the upper mold when the semiconductor wafer is sandwiched by the upper and the lower mold.

Claim 17 (original): A sealing apparatus as claimed in claim 12 wherein the shock absorber is a first shock absorber, further comprising:

a first block having a first recess, the lower mold being contained in the first recess;

a second block having a second recess, the first block being contained in the second recess; and

second shock absorbers, which are formed under the second block, buffering stress from the upper mold when the semiconductor wafer is sandwiched by the upper and the lower mold.

Claim 18 (original): A sealing apparatus as claimed in claim 16, wherein the second shock absorber is formed by a metallic compression spring.

Claim 19 (original): A sealing apparatus as claimed in claim 17, wherein each second shock absorber is formed by a metallic compression spring.

Claim 20 (original): A sealing apparatus as claimed in claim 13, wherein the shock absorbers are first shock absorbers, further comprising:

a first block having a first recess, the lower mold being contained in the first recess;

a second block having a second recess, the first block being contained in the second recess; and

a second shock absorber, which is formed under the second block, buffering stress from the upper mold when the semiconductor wafer is sandwiched by the upper and the lower mold.

Claim 21 (original): A sealing apparatus as claimed in claim 13, wherein the shock absorbers are first shock absorbers, further comprising:

a first block having a first recess, the lower mold being contained in the first recess;

a second block having a second recess, the first block being contained in the second recess; and

second shock absorbers, which are formed under the second block, buffering stress from the upper mold when the semiconductor wafer is sandwiched by the upper and the lower mold.

Claim 22 (original): A sealing apparatus as claimed in claim 20, wherein the second shock absorber is formed by a metallic compression spring.

Claim 23 (original): A sealing apparatus as claimed in claim 21, wherein each second shock absorber is formed by a metallic compression spring.

Claim 24 (original): A sealing apparatus as claimed in claim 1, wherein the upper mold includes a main surface and includes a cavity on the main surface, and wherein the semiconductor wafer is sandwiched at its periphery by the main surface of the upper mold other than an area where the cavity is formed and the lower mold whereby the resin is not formed on the periphery of the semiconductor wafer.

Claim 25 (original): A sealing apparatus as claimed in claim 24, wherein the cavity is located at a position corresponding to the area, wherein the upper mold further includes a gate connected to the cavity and cull connected to the gate, wherein the gate is located at a position corresponding the periphery of the semiconductor wafer, and where the cavity is formed deeper than the gate.

Claim 26 (original): A sealing apparatus as claimed in claim 25, wherein the width of the gate is expanding toward the cavity.

Claim 27 (original): A sealing apparatus as claimed in claim 25, wherein the upper mold includes a air vent, which is located at a position opposite to the gate, for releasing air in the cavity when the semiconductor wafer is sealed.

Claim 28 (original): A sealing apparatus as claimed in claim 26, wherein the upper mold includes a air vent, which is located at a position opposite to the gate, for releasing air in the cavity when the semiconductor wafer is sealed.

Claim 29 (original): A sealing apparatus as claimed in claim 24, further comprising a projection member being formed underneath the center of a back surface the lower mold, which is opposite to the uneven surface.

Claim 30 (original): A sealing apparatus as claimed in claim 24, further comprising ejection pins formed in the lower mold, the ejection pins pushing the semiconductor wafer up after the semiconductor wafer is sealed by the resin.

Claim 31 (original): A sealing apparatus as claimed in claim 30, wherein the ejection pins are disposed symmetrically against the center of the area.

Claim 32 (currently amended): A semiconductor device manufacturing mold for setting a semiconductor wafer having semiconductor elements on its surface in order to seal the surface by resin, comprising:

an upper mold; and

a lower mold having [[an]] a first area where the semiconductor wafer is to be mounted, wherein the lower mold ~~having~~ has an uneven surface ~~in the area~~ ,which is formed within a second area, which is in the first area, and wherein the uneven surface is not formed in the periphery of the first area.

Claim 33 (original): A semiconductor device manufacturing mold as claimed in claim 32, wherein the uneven surface is formed by an electric discharging process in coarse condition.

Claim 34 (cancelled).

Claim 35 (currently amended): A semiconductor device manufacturing mold ~~as claimed in claim 33,~~ for setting a semiconductor wafer having semiconductor elements on its surface in order to seal the surface by resin, comprising:

an upper mold; and

a lower mold having [[an]] area where the semiconductor wafer is to be mounted, the lower mold having an uneven surface in the area,

wherein the uneven surface has a roughness in a range between 8μm and 12μm.

Claim 36 (currently amended): A semiconductor device manufacturing mold as claimed in claim [[34]] 33, wherein the uneven surface has a roughness in a range between 8μm and 12μm.

Claim 37 (original): A semiconductor device manufacturing mold as claimed in claim 32, wherein the uneven surface is formed by slits.

Claim 38 (original): A semiconductor device manufacturing mold as claimed in claim 37, wherein the slits are formed in parallel to each other.

Claim 39 (original): A semiconductor device manufacturing mold as claimed in claim 37, wherein the area is a first area, the slits is formed within a second area, which is in the first area, and the slits are not extended to the periphery of the first area.

Claim 40 (original): A semiconductor device manufacturing mold as claimed in claim 38, wherein the area is a first area, the slits is formed within a second area, which is in the first area, and the slits are not extended to the periphery of the first area.

Claim 41 (original): A semiconductor device manufacturing mold as claimed in claim 32, wherein the uneven surface is formed by a single spiral slit.

Claim 42 (original): A semiconductor device manufacturing mold as claimed in claim 41, wherein the area is a first area, the single spiral slit is formed within a second area, which is in the first area, and the single spiral slit is not extended to the periphery of the first area.

Claim 43 (currently amended): A gate of a sealing device having a mold in which a semiconductor wafer having semiconductor elements on its surface is set in an area in order to form a resin layer on the semiconductor wafer by

introducing a melted resin from a resin supplier, wherein the mold includes an upper mold and a lower mold, the gate being formed in the upper mold when the upper mold and the lower mold are closed, and being arranged outside the area, the gate introducing the melted resin into the mold ~~from a part of a periphery of the semiconductor wafer, and~~ wherein a depth of the gate is getting deeper from an outer end toward the inner end, which is closer to the area ~~lower than the thickness of the resin layer~~.

Claim 44 (currently amended): A gate as claimed in claim 43, wherein a width of the gate is ~~expanding~~ getting expanded from ~~the resin supplier~~ the outer end toward ~~the semiconductor wafer~~ the inner end.

Claim 45 (currently amended): A sealing apparatus for sealing a semiconductor wafer having semiconductor elements on its surface by resin, comprising:

an upper mold;

a lower mold having an area where the semiconductor wafer is to be mounted; and

a shock absorber~~, which is formed under the lower mold,~~ buffering stress ~~from the upper mold when the semiconductor wafer is sandwiched by the upper and lower molds~~ to the semiconductor wafer, wherein a part of the shock absorber is exposed in the area.

Claim 46 (currently amended): A sealing apparatus for sealing a semiconductor wafer having semiconductor elements on its surface by resin, comprising:

an upper mold;

a lower mold having an area where the semiconductor wafer is to be mounted; and

shock absorbers~~, which are formed under the lower mold,~~ buffering stress ~~from the upper mold when the semiconductor wafer is sandwiched by the upper and the lower mold,~~ to the semiconductor wafer, wherein a part of each shock absorber is exposed in the area, and wherein the shock absorbers [[being]] are disposed symmetrically against the center of the area.

Claim 47 (original): A sealing apparatus as claimed in claim 45, wherein the shock absorber is formed by a metallic compression spring.

Claim 48 (original): A sealing apparatus as claimed in claim 46, wherein each shock absorber is formed by a metallic compression spring.

Claim 49 (currently amended): A sealing apparatus as claimed in claim 45, wherein the shock absorber is a first shock absorber, further comprising:

a first block having a first recess, the lower mold being contained in the first recess;

a second block having a second recess, the first block being contained in the second recess; and

a second shock absorber, which is formed under the second block, buffering stress ~~from the upper mold when the semiconductor wafer is sandwiched by the upper and the lower mold,~~ to the semiconductor wafer.

Claim 50 (currently amended): A sealing apparatus as claimed in claim 45, wherein the shock absorber is a first shock absorber, further comprising:

a first block having a first recess, the lower mold being contained in the first recess;

a second block having a second recess, the first block being contained in the second recess; and

second shock absorbers, which are formed under the second block, buffering stress ~~from the upper mold when the semiconductor wafer is sandwiched by the upper and the lower mold,~~ to the semiconductor wafer.

Claim 51 (original): A sealing apparatus as claimed in claim 49, wherein the second shock absorber is formed by a metallic compression spring.

Claim 52 (original): A sealing apparatus as claimed in claim 50, wherein each second shock absorber is formed by a metallic compression spring.

Claim 53 (currently amended): A sealing apparatus as claimed in claim 46, wherein the shock absorbers are first shock absorbers, further comprising:

a first block having a first recess, the lower mold being contained in the first recess;

a second block having a second recess, the first block being contained in the second recess; and

a second shock absorber, which is formed under the second block, buffering stress ~~from the upper mold when the semiconductor wafer is sandwiched by the upper and the lower mold,~~ to the semiconductor wafer.

Claim 54 (currently amended): A sealing apparatus as claimed in claim 46, wherein the shock absorbers are first shock absorbers, further comprising:

a first block having a first recess, the lower mold being contained in the first recess;

a second block having a second recess, the first block being contained in the second recess; and

second shock absorbers, which are formed under the second block, buffering stress ~~from the upper mold when the semiconductor wafer is sandwiched by the upper and the lower mold,~~ to the semiconductor wafer.

Claim 55 (original): A sealing apparatus as claimed in claim 53, wherein the second shock absorber is formed by a metallic compression spring.

Claim 56 (original): A sealing apparatus as claimed in claim 54, wherein each second shock absorber is formed by a metallic compression spring.

Claims 57-91 (cancelled):

Claim 92 (new): A sealing apparatus as claimed in claim 4, wherein the uneven surface is formed by an electric discharging process in coarse condition.

Claim 93 (new): A sealing apparatus as claimed in claim 35, wherein the uneven surface is formed by an electric discharging process in coarse condition.